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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,330	01/30/2004	Philip B. James-Roxby	X-1557-2 US	7401

24309 7590 07/01/2009

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EXAMINER	
SEYE, ABDOU K	

ART UNIT	PAPER NUMBER
2194	

MAIL DATE	DELIVERY MODE
07/01/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/769,330	JAMES-ROXBY ET AL.	
	Examiner	Art Unit	
	Abdou Karim Seye	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/02/2009, 04/29/2009, 04/21/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are pending in this application.

Claim Objections

2. Claim 20 is objected because of the following informality:

In line 1 of the claim, "claim 29" appears to be typographical error of --claim 19--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103 (a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-20 are rejected under 35 U.S.C. 103 (a) as unpatentable over He et al. (US 20020120912) in view of Ohnishi (US 20020188923).

5. As to claim 1 , He teaches the invention substantially as claimed including a

method for multithread processing of messages using an integrated circuit (abstract; FIG. 1), comprising:

configuring configurable logic of said integrated circuit to have a plurality of thread circuits (FIG. 1; paragraph 35; paragraph 23) and an interconnection topology amongst said plurality of thread circuits (paragraph 22-23);

concurrently processing messages using said plurality of thread circuits (paragraph 37; wherein "the multithreaded parallelism" are known to include concurrent processing of threads).

6. He does not explicitly teach each of said plurality of thread circuits providing a control signal to each other of said plurality of thread circuits through said interconnection topology and controlling operation of at least one thread circuit of said plurality of thread circuits in accordance with control data respective control signal from at least one other thread circuit of said plurality of thread circuits over said interconnection topology.

7. Ohnishi teaches a thread circuit providing control signal to another thread circuit (FIG. 17; paragraph 37); and control operation of a thread circuit controlling data path/data of the control signal ("N3e", FIG. 16; paragraph 28-28; paragraph 38). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify He 's invention with Ohnishi's to have plurality of thread circuits providing a control signal to each other of said plurality of thread circuits through said

interconnection topology and controlling operation of at least one thread circuit of said plurality of thread circuits in accordance with control data respective control signal from at least one other thread circuit of said plurality of thread circuits over said interconnection topology , because it would improve the efficiency of He's system by allowing the increase in quality and quantity of data communication between thread circuits .

8. As to claim 2, Ohnishi teaches, wherein each of said plurality of thread circuits comprises a state machine (abstract; paragraph 36),

9. As to claim 3, Ohnishi teaches, wherein said integrated circuit is a programmable logic device (abstract; paragraph 2), and wherein said state machine of each of said plurality of thread circuits is implemented using programmable logic blocks of said integrated circuit (FIG. 9A/B);

10. As to claim 4, Ohnishi teaches, wherein said controlling step comprises: activating said at least one thread in response to said control data comprising a start command (paragraph 53); deactivating said at least one thread in response to said control data comprising a stop command (paragraph 102) ; and suspending said at

least one thread in response to said control data comprising a suspend command (abstract; wherein the "wait state" is the suspending command).

11. As to claim 5, Ohnishi teaches, wherein said control data comprises status data associated with said at least one other thread circuit of said plurality of thread circuits (paragraph 36-37).

12. As to claim 6, He teaches, further comprising: communicating data from a first thread circuit of said plurality of thread circuits to a second thread circuit of said plurality of thread circuits through said interconnection topology (abstract; paragraph 23 and 48).

13. As to claim 7, He teaches the invention substantially as claimed including a method of implementing multithread processing of messages using an integrated circuit (abstract; FIG. 1), comprising:

specifying a plurality of threads for concurrently processing messages (paragraph 23 and 37) ;

specifying an interconnection topology amongst said plurality of threads (paragraph 22-23 and 44), at least a portion of said interconnection topology including a connection between said at least one thread and said at least one other thread (paragraph 23); and

generating a physical description of a multithreading system in response to said plurality of threads and said interconnection topology (FIG. 1; paragraph 35), said physical description being defined in terms of components of said integrated circuit (paragraph 37).

14. He does not explicitly teach explicitly that threads including control logic for controlling operation of at least one other thread of said plurality of threads and said connection including at least one control signal provided by said control logic .

15. Ohnishi teaches a thread circuit providing control signal to another thread circuit (FIG. 17; paragraph 37); and control operation of a thread circuit controlling data path/data of the control signal ("N3e", FIG. 16; paragraph 28-28; paragraph 38). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify He 's invention with Ohnishi's to have plurality of thread circuits providing a control signal to each other of said plurality of thread circuits through said interconnection topology and controlling operation of at least one thread circuit of said plurality of thread circuits in accordance with control data respective control signal from at least one other thread circuit of said plurality of thread circuits over said interconnection topology , because it would improve the efficiency of He's system by allowing the increase in quality and quantity of data communication between thread circuits .

16. As to claim 8, He teaches, processing said physical description to generate data for configuring said integrated circuit with said multithreading system (abstract).

17. As to claim 9, Ohnishi teaches, wherein said physical description comprises a hardware description language description (paragraph 144).

18. As to claim 10, it is rejected for the same reasons as claim 4 above.

19. As to claim 11, it is rejected for the same reasons as claim 6 above.

20. As to claim 12, Ohnishi teaches, wherein said data is communicated in accordance with a data validity flag (paragraph 37).

21. As to claim13, Ohnishi teaches, wherein said data is communicated in accordance with a request generated by said second thread (paragraph 38).

22. As to claim 14, He teaches the invention substantially as claimed including a design tool (101, FIG. 1; wherein the "GUI" is the design tool) for implementing a

multithread message processing system using an integrated circuit (abstract) , comprising:

means for specifying attributes of said multithread message processing system (paragraph 35; wherein the GUI is used for specifying information/attributes);

a first database for storing a multithread model having a thread model and an interconnection model (103; FIG. 1; paragraph 36; wherein the database is the first storage; paragraph 20; wherein the "cell of the IC design" is the thread model; paragraph 22; wherein the "group of interconnections" is the interconnection model); and

a multithread model section (paragraph 37; wherein the multithreaded parallelism is the model), comprising:

means for generating a plurality of instances of said thread model (paragraph 20; wherein the "first cell instance and second cell instance" are the plurality of instances) and an instance of said interconnection model in response to said specified attributes (paragraph 22; wherein the" first group of interconnections" is the instance of the interconnection model); and

means for implementing said plurality of thread model instances and said interconnection model instance in terms of said integrated circuit architecture (abstract; paragraph 50).

23. He does not explicitly teach a second data base for storing an architecture of said integrated circuit . However He teaches files/database in (paragraph 36) wherein cells/ thread instances, and interconnections/ interconnection model instances are described in. it would be obvious to a person of ordinary skilled in the art at the time the invention was made to have a second database for storage of the threads and interconnections instances, because it would increase the efficiency of He's system, by allowing data to be accessed and retrieved more efficiently.

24. As to claim 15, He does not explicitly teach a third data base for storing a set of primitive, it would be obvious to a person of ordinary skilled in the art to have a third database for storing a set of primitives and to defined the attributes in accordance with said primitives, because it would increase the efficiency of He's system, by allowing fast access and retrieval of data in order to improve the He's system efficiency.

25. As to claim 16, it is rejected for the same reasons as claim 2 above.

26. As to claim 17, it is rejected for the same reasons as claim 3 above.

27. As to claim 18, it is rejected for the same reasons as claim 7 above.

28. As to claim 19-20, they are rejected for the same reasons as claim 3 above.

Response to Arguments

29. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

30. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abdou Karim Seye whose telephone number is 571-270-1062. The examiner can normally be reached on Monday - Friday 8:30 - 6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sough Hyung can be reached on (571)272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hyung S. SOUGH/
Supervisory Patent Examiner, Art Unit 2194
06/29/09

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